IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) An integrated circuit for a wireless communication device, comprising:

an always-on power domain including circuit blocks coupled to a first power supply and powered on at all times while the wireless device is powered on; and

at least one collapsible power domain, each collapsible power domain including circuit blocks coupled to a second power supply via a respective power connection and powered on or off by the power connection, wherein the always-on power domain determines power on and off states of all of the at least one collapsible power domain and further independently determines power on and off state of each of the at least one collapsible power domain.

2. (Original) The integrated circuit of claim 1, wherein the circuit blocks in the at least one collapsible power domain are operable to perform modulation and demodulation for wireless communication.

3. (Original) The integrated circuit of claim 1, wherein the always-on power domain is operable to maintain a timeline for each of at least one wireless communication system, the timeline for each system indicating sleep times and on-line times for the wireless device with respect to the system, the sleep times corresponding to times that the wireless device does not receive messages from the system, and the on-line times corresponding to times that the wireless device processes a signal for the system.

4. (Original) The integrated circuit of claim 3, wherein the at least one collapsible power domain is powered off during the sleep times when the wireless device is not receiving messages from any one of the at least one wireless communication system.

5. (Original) The integrated circuit of claim 1, wherein the power connection for each collapsible power domain includes at least one switch operable to provide power to the

circuit blocks in the power domain when enabled and to remove power from the circuit blocks when disabled.

6. (Original) The integrated circuit of claim 5, wherein the at least one switch for each power connection comprises a headswitch or a footswitch.

7. (Original) The integrated circuit of claim 1, wherein the first and second power supplies are one common power supply.

8. (Original) The integrated circuit of claim 1, wherein the first and second power supplies are different power supplies with different voltages.

9. (Original) The integrated circuit of claim 1, wherein the always-on power domain includes a power controller operable to provide at least one control signal to power on or off each of the at least one collapsible power domain.

10. (Original) The integrated circuit of claim 1, wherein the always-on power domain includes an interrupt controller operable to monitor input signals for the integrated circuit and to provide an indication to power on the at least one collapsible power domain if required by the input signals.

11. (Original) The integrated circuit of claim 3, wherein the always-on power domain includes a sleep controller operable to maintain the timeline for each of the at least one wireless communication system.

12. (Original) The integrated circuit of claim 1, wherein the always-on power domain includes a clock controller operable to enable and disable clocks for the at least one collapsible power domain.

13. (Original) The integrated circuit of claim 1, further comprising:

at least one output circuit for at least one output pin of the integrated circuit, one output circuit for each output pin, each output circuit receiving an output signal from one of

the at least one collapsible power domain and driving the associated output pin with the output signal.

14. (Original) The integrated circuit of claim 13, wherein each output circuit includes a latch operable to maintain logic state of the output signal for the associated output pin while the associated collapsible power domain is powered off.

15. (Original) The integrated circuit of claim 1, further comprising:

at least one interface circuit for at least one connection between the always-on power domain and the at least one collapsible power domain, one interface circuit for each connection between two power domains, each interface circuit including a clamping circuit operable to clamp a respective interface signal to logic low or high.

16. (Original) The integrated circuit of claim 15, wherein each interface circuit further includes a level shifter operable to translate the respective interface signal between two different voltages for the two power domains.

17. (Original) The integrated circuit of claim 1, wherein the power connection for each collapsible power domain includes a sufficient number of electrostatic discharge (ESD) diodes to prevent shorting of the second power supply when the collapsible power domain is powered off.

18. (Original) The integrated circuit of claim 1, further comprising:

an internal memory operable to receive boot code for configuring a memory system for the integrated circuit.

19. (Currently amended) An integrated circuit for a wireless communication device, comprising:

an always-on power domain including circuit blocks coupled to a first power supply and powered on at all times while the wireless device is powered on;

at least one collapsible power domain, each collapsible power domain including circuit blocks coupled to a second power supply via a respective power connection and

powered on or off by the power connection, wherein the always-on power domain determines power on and off states of all of the at least one collapsible power domain and further independently determines power on and off state of each of the at least one collapsible power domain; and

an internal memory operable to receive boot code for configuring a memory system for the integrated circuit, wherein the boot code is downloaded from an external non-volatile memory to the internal memory and executed when the at least one collapsible power domain is powered on.

20. (Currently amended) An integrated circuit for a wireless communication device, comprising:

an always-on power domain including circuit blocks coupled to a first power supply and powered on at all times while the wireless device is powered on;

at least one collapsible power domain, each collapsible power domain including circuit blocks coupled to a second power supply via a respective power connection and powered on or off by the power connection, wherein the always-on power domain determines power on and off states of all of the at least one collapsible power domain and further independently determines power on and off state of each of the at least one collapsible power domain; and

an internal memory operable to receive boot code for configuring a memory system for the integrated circuit, wherein the boot code, when executed, configures a memory controller for the memory system and sets up an external volatile memory.

21. (Original) The integrated circuit of claim 1, wherein the wireless device is operable to communicate with a Code Division Multiple Access (CDMA) system.

22. (Original) The integrated circuit of claim 1, wherein the wireless device is operable to communicate with a Global System for Mobile Communications (GSM) system.

23. (Currently amended) A wireless communication device comprising a modem processor operable to perform modulation and demodulation for wireless communication, the modem processor including

an always-on power domain including circuit blocks coupled to a first power supply and powered on at all times while the wireless device is powered on, and

at least one collapsible power domain, each collapsible power domain including circuit blocks coupled to a second power supply via a power connection and powered on or off by the power connection, wherein the always-on power domain determines power on and off states of all of the at least one collapsible power domain and further independently determines power on and off state of each of the at least one collapsible power domain.

24. (Original) The wireless device of claim 23, wherein the always-on power domain is operable to maintain a timeline for each of at least one wireless communication system, the timeline for each system indicating sleep times and on-line times for the wireless device with respect to the system, the sleep times corresponding to times that the wireless device does not received messages from the system, and the on-line times corresponding to times that the wireless device processes a signal for the system, and wherein the at least one collapsible power domain is powered off during the sleep times for the at least one system.

25. (Original) The wireless device of claim 23, further comprising:

a main oscillator operable to provide a main clock used by circuit blocks in the modem processor while the at least one collapsible power domain is powered on; and

a sleep oscillator operable to provide a sleep clock used by the circuit blocks in the always-on power domain while the at least one collapsible power domain is powered off, wherein the sleep clock has a lower frequency than the main clock.

26. (Original) The wireless device of claim 23, further comprising:

a volatile memory operable to store program code for the wireless device, wherein the volatile memory is placed in a self-refresh mode when not accessed by any collapsible power domain.

27. (Currently amended) A method of conserving power for a wireless communication device, the method comprising:

powering on circuit blocks in an always-on power domain at all times while the wireless device is powered on;

powering on or off circuit blocks in each of at least one collapsible power domain via a power connection for the collapsible power domain; and

determining power on and off states of all of the at least one collapsible power domain and independently for each of the at least one collapsible power domain with the always-on power domain.

28. (Original) The method of claim 27, further comprising:

receiving an indication to enter sleep, and wherein the circuit blocks in the at least one collapsible power domain are powered off during sleep exceeding a particular time duration.

29. (Original) The method of claim 27, further comprising:

latching logic states of output pins prior to powering off the at least one collapsible power domain; and

releasing the output pins after powering on the at least one collapsible power domain.

30. (Original) The method of claim 27, further comprising:

saving hardware states prior to powering off the at least one collapsible power domain; and

restoring the hardware states after powering on the at least one collapsible power domain.

31. (Original) The method of claim 27, further comprising:

placing a volatile memory in a self-refresh mode prior to powering off the at least one collapsible power domain; and

taking the volatile memory out of the self-refresh mode after powering on the at least one collapsible power domain.

32. (Original) The method of claim 27, further comprising:

disabling clocks for the at least one collapsible power domain prior to powering off the at least one collapsible power domain; and

enabling the clocks after powering on the at least one collapsible power domain.

33. (Original) The method of claim 27, further comprising:

powering off an oscillator used to generate the clocks for the at least one collapsible power domain prior to powering off the at least one collapsible power domain; and

powering on the oscillator after powering on the at least one collapsible power domain.

34. (Currently amended) An apparatus for wireless communication, comprising

means for powering on circuit blocks in an always-on power domain at all times while the apparatus is powered on;

means for powering on or off circuit blocks in each of at least one collapsible power domain via a power connection for the collapsible power domain; and

means for determining power on and off states of all of the at least one collapsible power domain and independently for each of the at least one collapsible power domain with the always-on power domain.

35. (Original) The apparatus of claim 34, further comprising:

means for receiving an indication to enter sleep, and wherein the circuit blocks in the at least one collapsible power domain are powered off during sleep.

36. (Original) The apparatus of claim 34, further comprising:

means for latching logic states of output pins prior to powering off the at least one collapsible power domain; and

means for releasing the output pins after powering on the at least one collapsible power domain.

37. (Currently amended) The integrated circuit of claim 1, wherein the always-on power domain ~~independently determines power on and off state of~~ maintains a finite state machine for each of the at least one collapsible power domain.

38. (Previously presented) The integrated circuit of claim 1, wherein the always-on power domain performs a power down sequence to power down the at least one collapsible power domain.

39. (Previously presented) The integrated circuit of claim 1, wherein the always-on power domain performs a power up sequence to power up the at least one collapsible power domain.